1. A process for forming a contact opening to a semiconductor material, said process comprising:

forming a substantially undoped silicon dioxide layer over a layer of semiconductor material;

forming a doped silicon dioxide layer over said undoped silicon dioxide layer; and

selectively removing a portion of said doped silicon dioxide layer at a material removal rate that is at least 10 times higher for doped silicon dioxide than for undoped silicon dioxide or for said layer of semiconductor material to form an opening extending to a contact surface on said layer of semiconductor material.

2. A process as recited in Claim 1, wherein selectively removing said doped silicon dioxide layer comprises:

forming a layer of photoresist over said doped silicon dioxide layer;

patterning said layer of photoresist; and

etching said doped silicon dioxide layer through the pattern of said layer of photoresist.

3. A process as recited in Claim 1, wherein the semiconductor material is monocrystalline silicon.

4. A process as recited in Claim 1, wherein selectively removing said doped silicon dioxide layer comprises a plasma etching process for etching said doped silicon dioxide layer in a plasma etcher.

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5. A process as recited in Claim 4, wherein said plasma etching process has a plasma density in a range from about 10^9 /cm^3 to about 10^{13} /cm^3 -

6. A process as recited in Claim 4, wherein said plasma etching process is conducted in a pressure range from about 1 millitorr to about 400 millitorr.

7. A process as recited in Claim 4, wherein during said plasma etching process said reactor cathode has a temperature range from about 10°C to about 80°C.

8. A process as recited in Claim 4, wherein the temperature range of the semiconductor material during said plasma etching process is from about 40°C to about 130°C.

9. A process as defined in Claim 1, wherein selectively removing said doped silicon dioxide layer comprises etching of said doped silicon dioxide with an etchant selected from the group consisting of C_2F_6, CF_4, C_3F_8, C_4F_{10}, C_5F_8, CH_2F_2, CHF_3, C_2HF_5, and CH_3F.

10. A process as defined in Claim 9, wherein selectively removing said doped silicon dioxide layer comprises etching of said doped silicon dioxide with an etchant selected from the group consisting of CH_2F_2 and CH_3F.

11. A process as recited in Claim 1, wherein selectively removing said doped silicon dioxide layer comprises etching of said doped silicon dioxide with a fluorinated chemical etchant.

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12. A process as recited in Claim 1, wherein said doped silicon dioxide layer is selected from the group consisting of BPSG, PSG, and BSG.

13. A process for forming contact to a semiconductor material, said process comprising:

forming a substantially undoped silicon dioxide layer over a layer of monocrystalline silicon;

forming a doped silicon dioxide layer over said undoped silicon dioxide layer, said doped silicon dioxide layer being selected from the group consisting of BPSG, PSG, and BSG;

forming a layer of photoresist over said doped silicon dioxide layer;

patterning said layer of photoresist;

etching said doped silicon dioxide layer through the pattern of said layer of photoresist in a plasma etching process in a plasma etcher, said plasma etching process being conducted:

at a pressure range from about 1 millitorr to about 400 millitorr;

a temperature range of the cathode that is from about 10°C to about 80°C;

in a plasma density in a range from about 10^9 /cm^3 to about 10^{13} /cm^3

with a fluorinated chemical etchant; and

whereby a contact is exposed on said layer of monocrystalline silicon.

14. A process as recited in Claim 13, wherein the temperature range of the semiconductor material during said plasma etching process is from about 40°C to about 130°C.

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15. A process as recited in Claim 13, wherein said fluorinated chemical etchant comprises an etchant selected from the group consisting of C_2F_6, CF_4, C_3F_8, C_4F_{10}, C_5F_8, CH_2F_2, CHF_3, C_2HF_5, and CH_3F.

16. A process as defined in Claim 15, wherein selectively removing said doped silicon dioxide layer comprises etching of said doped silicon dioxide with an etchant selected from the group of CH_2F_2 and CH_3F.

17. A process as recited in Claim 13, wherein said plasma etching process is conducted at a material removal rate that is at least 10 times higher for doped silicon dioxide than for undoped silicon dioxide or for said semiconductor material.

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18. A process for forming a contact to a semiconductor substrate comprising:

providing a gate oxide layer over the semiconductor substrate;

providing a pair of gate stacks in spaced relation to one another on the semiconductor substrate, each of said gate stacks having at least one conductive layer formed therein and a substantially undoped silicon dioxide layer extending over said conductive layer;

forming a spacer adjacent to each of said gate stacks;

forming a doped silicon dioxide layer over said pair of gate stacks and over said exposed surface on said semiconductor substrate;

selectively removing a portion of said doped silicon dioxide layer between said pair of gate stacks to expose said surface on said semiconductor substrate, while removing substantially less of said undoped silicon dioxide layer over said pair of gate stacks, wherein said etching removes doped silicon dioxide at a material removal rate that is at least 10 times higher than for each of undoped silicon dioxide, the spacer material the spacer material, and the semiconductor substrate.

19. A process as recited in Claim 18, further comprising:

forming polysilicon layer over said gate oxide layer;

forming a refractory metal silicide layer over said polysilicon layer; and

forming a substantially undoped silicon dioxide layer over said refractory metal silicide layer.

20. A process as recited in Claim 19, further comprising selectively removing portions of said substantially undoped silicon dioxide layer, said refractory metal silicide layer, said polysilicon layer, and said gate oxide layer.

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21. A process as recited in Claim 18, wherein said gate stack comprises:

said substantially undoped silicon dioxide layer as the top layer thereof;

a refractory metal silicide layer;

a polysilicon layer; and

a gate oxide layer as the bottom layer thereof.

22. A process as recited in Claim 18, wherein the spacer material is substantially composed of silicon nitride.

23. A process as recited in Claim 18, wherein the spacer material is composed of substantially undoped silicon dioxide.

24. A process as recited in Claim 18, wherein the semiconductor material is monocrystalline silicon.

25. A process as recited in Claim 18, wherein said plasma etcher is selected from the group consisting of an RF RIE etcher, a MERIE etcher, and a high density plasma etcher.

26. A process as recited in Claim 18, further comprising the step of forming a contact plug composed of a conductive material and situated between said pair of gate stacks and over said surface on said semiconductor substrate.

27. A process as recited in Claim 21, wherein said refractory metal silicide layer is tungsten silicide.

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28. A process as recited in Claim 18, wherein said doped silicon dioxide layer is selected from the group consisting of BPSG, PSG, and BSG.

29. A process as recited in Claim 18, wherein selectively removing said doped silicon dioxide layer comprises:

forming a layer of photoresist over said doped silicon dioxide layer;

patterning said layer of photoresist; and

etching said doped silicon dioxide layer through the pattern of said layer of photoresist in a plasma etching process in a plasma etcher, said plasma etching process being conducted:

at a pressure range from about 1 millitorr to about 400 millitorr;

a temperature range of reactor cathode that is from about 10°C to about 80°C;

a temperature range of the semiconductor material is from about 40°C to about 130°C;

in a plasma density in a range from about 10^9 /cm^3 to about 10^{13} /cm^3 and

with a fluorinated chemical etchant.

30. A process as recited in Claim 29, wherein said fluorinated chemical etchants is selected from the group consisting of C_2F_6, CF_4, C_3F_8, C_4F_{10}, C_5F_8, CH_2F_2, CHF_3, C_2HF_5, and CH_3F.

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31. A process for forming a contact to a semiconductor material comprising:

depositing a gate oxide layer over a layer of silicon of a semiconductor substrate;

depositing a polysilicon layer over said gate oxide layer;

depositing a refractory metal silicide layer over said polysilicon layer;

depositing a substantially undoped silicon dioxide layer over said refractory metal silicide layer;

selectively removing portions of said substantially undoped silicon dioxide layer, said refractory metal silicide layer, said polysilicon layer, and said gate oxide layer so as to form a pair of gate stacks separated by an exposed portion of said silicon layer, each said gate stack having a lateral side substantially perpendicular to said gate oxide layer and being composed of:

said substantially undoped silicon dioxide layer as the top layer thereof;

said refractory metal silicide layer;

said polysilicon layer; and

said gate oxide layer as the bottom layer thereof;

forming a spacer on the lateral side of each said gate stack from a layer of spacer material;

depositing a doped silicon dioxide layer over said pair of gate stacks and over said exposed portion of said silicon layer, said doped silicon dioxide layer being is selected from the group consisting of BPSG, PSG, and BSG; and

etching said doped silicon dioxide layer with a plasma etching system having a plasma density in a range from about 10^9 /cm^3 to about 10^{13} /cm^3 in an etcher selected from a group consisting of RF RIE, MERIE plasma etching system, and high density plasma etching system, said plasma etching system having a pressure range

from about 1 millitorr to about 400 millitorr, said doped silicon dioxide layer being etched between said pair of gate stacks so as to expose said exposed portion of said silicon layer, said etching having a material removal rate that is at least 10 times higher for doped silicon dioxide than for undoped silicon dioxide, said spacer material, or silicon, said etching of said doped silicon dioxide being conducted with a fluorinated chemical etchant.

32. A process as recited in Claim 31, wherein the spacer material is substantially composed of one of silicon nitride and substantially undoped silicon dioxide.

33. A process as recited in Claim 31, further comprising forming a contact plug composed of a conductive material and situated between said pair of gate stacks and over the exposed portion of said silicon layer.

34. A process as recited in Claim 34, wherein said fluorinated chemical etchant is selected from the group consisting of C_2F_6, CF_4, C_3F_8, C_4F_{10}, C_2F_8, CH_2F_2, CHF_3, C_2HF_5, and CH_3F.

35. A process as recited in Claim 31, wherein during etching of said doped silicon dioxide layer with said plasma etching system, the temperature range of said reactor cathode is from about 10°C to about 80°C.

36. A process as recited in Claim 31, wherein the temperature range of the semiconductor material during said plasma etching process is from about 40°C to about 130°C.

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37. A process for forming a gate structure comprising:

providing a multilayer structure comprising a layer of silicon dioxide over a layer of silicon;

depositing a layer of substantially undoped silicon dioxide over said multilayer structure using a precursor having a gaseous silane, hydrogen, and oxygen flow;

forming a first layer of photoresist over said layer of undoped silicon dioxide;

patterning said first photoresist layer to form a first pattern;

etching said layer of undoped silicon dioxide and said multilayer structure through said first pattern to expose a contact surface on at least a portion of said layer of silicon;

depositing a layer of a nonconductive material over said layer of undoped silicon dioxide and said contact surface on said layer of silicon;

etching said layer of said nonconductive material to thereby create a spacer over a lateral side of said layer of undoped silicon dioxide and over a lateral side of said multilayer structure, said spacer being generally perpendicular to said layer of silicon;

removing said first layer of photoresist;

depositing a doped silicon dioxide layer over said multilayer structure;

forming a said second layer of photoresist over said layer of doped silicon dioxide;

patterning said second layer of photoresist to form a second pattern;

etching said layer of doped silicon dioxide and said multilayer structure with a carbon fluorine etch through said second pattern to expose said contact surface on said layer of silicon, said etching having a material removal rate that is at least

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10 times greater for doped silicon dioxide than for substantially undoped silicon dioxide, photoresist, or nonconductive material;

removing said second layer of photoresist; and

forming a contact plug composed of a conductive material in contact with said contact surface on said layer of silicon.

38. A process as recited in Claim 37, wherein said nonconductive material is one of silicon nitride and substantially undoped silicon dioxide.

39. A process as recited in Claim 37, wherein said carbon fluorine etch is an anisotropic plasma etch using fluorinated chemical etchants selected from a group consisting of C_2F_6, CF_4, C_3F_8, C_4F_{10}, C_5F_8, CH_2F_2, CHF_3, C_2HF_5, and CH_3F.

40. A process as recited in Claim 37, wherein said multilayer structure further comprises layers of gate oxide, polysilicon, and refractory metal silicide.

41. A process as recited in Claim 37, wherein said doped silicon dioxide layer is selected from a group consisting of BPSG, PSG, and BSG.

42. A process as recited in Claim 37, wherein etching said layer of doped silicon dioxide and said multilayer structure with a carbon fluorine etch utilizes a plasma etching system selected from a group consisting of RF RIE, MERIE system, and a high density plasma etch system.

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43. A process as recited in Claim 37, wherein etching said layer of doped silicon dioxide and said multilayer structure with a carbon fluorine etch is a plasma etching process being conducted:

at a pressure range from about 1 millitorr to about 400 millitorr;

a temperature range of reactor cathode that is from about 10°C to about 80°C;

a temperature range of the semiconductor material is from about 40°C to about 130°C;

in a plasma density in a range from about 10^9/cm3 to about 10^{13}/cm3; and

with a fluorinated chemical etchant.

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44. A process for forming a gate structure comprising:

providing a multilayer structure situated over a layer of silicon and comprising layers of gate oxide, polysilicon, and refractory metal silicide;

depositing a layer of substantially undoped silicon dioxide over said multilayer structure using a precursor having a gaseous silane, hydrogen, and oxygen flow;

forming a first layer of photoresist over said layer of undoped silicon dioxide;

patterning said first photoresist layer to form a first pattern;

etching said layer of undoped silicon dioxide and said multilayer structure through said first pattern to expose a contact surface on at least a portion of said layer of silicon;

removing said first layer of photoresist;

depositing a layer of a nonconductive material over said layer of undoped silicon dioxide and said contact surface on said layer of silicon;

etching said layer of said nonconductive material to thereby create a spacer over a lateral side of said layer of undoped silicon dioxide and over a lateral side of said multilayer structure, said spacer being generally perpendicular to said layer of silicon;

depositing a doped silicon dioxide layer over said multilayer structure and over said contact surface on said layer of silicon, wherein said doped silicon dioxide layer is selected from a group consisting of BPSG, PSG, and BSG;

forming a said second layer of photoresist over said layer of doped silicon dioxide;

patterning said second layer of photoresist to form a second pattern;

etching said layer of doped silicon dioxide and said multilayer structure with a carbon fluorine etch through said second pattern to expose said contact surface on

said layer of silicon, said etching having a material removal rate that is at least 10 times greater for doped silicon dioxide than for substantially undoped silicon dioxide, photoresist, or nonconductive material, wherein said carbon fluorine etch is an anisotropic plasma etch using a fluorinated chemical etchant, wherein said etching of said doped silicon dioxide utilizes a plasma etching system having a plasma density in a range from about 10^9 /cm^3 to about 10^{13} /cm^3 at a pressure in a range from about 1 millitorr to about 400 millitorr, the temperature range of said reactor cathode during said plasma etch being about 10°C to about 80°C, and the temperature range of the semiconductor material during said plasma etch being in the range of about 40°C to about 130°C;

removing said second layer of photoresist; and

forming a contact plug composed of a conductive material in contact with said contact surface on said layer of silicon.

45. A process as recited in Claim 44, wherein said fluorinated chemical etchant is selected from a group consisting of C_2F_6, CF_4, C_3F_8, C_4F_{10}, C_2F_8, CH_2F_2, CHF_3, C_2HF_5, and CH_3F.

46. A process as recited in Claim 44, wherein said nonconductive material is one of silicon nitride and substantially undoped silicon dioxide.

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47. A gate structure comprising:

a pair of gate stacks situated over a base silicon layer, each said gate stack comprising:

a gate oxide layer on said base silicon layer;

a polysilicon gate layer on said gate oxide layer;

a layer of refractory metal silicide on said polysilicon gate layer;

a substantially undoped silicon dioxide cap on said layer of refractory metal silicide;

a spacer in contact with a lateral side of each said gate stack and with said base silicon layer, said spacer being composed of a nonconductive material, each said lateral side of each said gate stack being substantially perpendicular to said base silicon layer;

a contact plug in contact with said base silicon layer composed of a conductive material, and being situated between said pair of gate stacks; and

a layer of doped silicon dioxide over said spacer, over said substantially undoped silicon dioxide cap, and in contact with said contact plug.

48. A gate structure as recited in Claim 47, wherein said nonconductive material is substantially composed of silicon nitride.

49. The gate structure as recited in Claim 47, wherein said nonconductive material is substantially composed of substantially undoped silicon dioxide, and each said spacer is integral with a respective one of said substantially undoped silicon dioxide cap.

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50. A method of forming a self-aligned contact, said method comprising:

providing a pair of gate stacks in spaced apart relation to one another on said semiconductor substrate, each of said gate stacks being covered by a substantially undoped silicon dioxide layer;

forming a spacer adjacent to each of said gate stacks;

forming a doped silicon dioxide layer over said pair of gate stacks and over said semiconductor substrate;

forming a layer of photoresist over said silicon dioxide layer;

patterning said layer of photoresist; and

selectively removing a portion of said doped silicon dioxide layer between said pair of gate stacks to expose a contact surface on said semiconductor substrate through said pattern of said layer of photoresist, while removing substantially less of said undoped silicon dioxide layer over said pair of gate stacks than doped silicon photoresist, said undoped silicon layer being capable of resisting said selective removal process thereby causing said selective removal process to be self-aligning between said pair of gate stacks.

51. A method as recited in Claim 50, wherein said selective removal of said doped silicon dioxide layer comprises etching said doped silicon dioxide layer in a plasma etching process being conducted:

at a pressure range from about 1 millitorr to about 400 millitorr;

a temperature range of the cathode that is from about 10°C to about 80°C;

in a plasma density in a range from about 10^9 /cm^3 to about 10^{13} /cm^3 and

with a fluorinated chemical etchants.

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52. A method as recited in Claim 51, wherein the temperature range of the semiconductor material during said plasma etching process is from about 40°C to about 130°C.

53. A method as recited in Claim 51, wherein said fluorinated chemical etchant comprises an etchant selected from the group consisting of C_2F_6, CF_4, C_3F_8, C_4F_{10}, C_2F_8, CH_2F_2, CHF_3, C_2HF_5, and CH_3F.

54. A method as recited in Claim 50, wherein said plasma etching process is conducted at a material removal rate that is at least 10 times higher for doped silicon dioxide than for undoped silicon dioxide or for semiconductor material.

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